WHAT IS CLAIMED IS:

1. Semiconductor equipment comprising:

a semiconductor substrate;

a plurality of transistors having a source cell and a drain cell disposed alternately on the substrate so as to form a mesh pattern; and

upper and lower layer wirings for electrically connecting the source cells and the drain cells,

wherein the lower layer wiring includes a first source wiring having a plurality of stripes for connecting the neighboring source cells and a first drain wiring having a plurality of stripes for connecting the neighboring drain cells,

wherein the upper layer wiring includes a second source wiring having a plurality of stripes for connecting to the first source wiring and a second drain wiring having a plurality of stripes for connecting to the first drain wiring,

wherein the second source wiring has a width of the stripe, which is wider than that of the first source wiring, and the second drain wiring has a width of the stripe, which is wider than that of the first drain wiring, and

wherein the stripes of the second source wiring and the second drain wiring are disposed alternately.

2. The semiconductor equipment according to claim 1,

wherein the transistor is a lateral type metal oxide semiconductor transistor, and the source and drain cells are disposed on a principal plane of the substrate,

wherein the upper and lower layer wirings are disposed on the substrate,

wherein the first source wiring connects the neighboring source cells disposed in a diagonal direction of the mesh pattern, and the first drain wiring connects the neighboring drain cells disposed in the diagonal direction,

wherein the second source wiring is disposed perpendicularly to the lower layer wiring, and connects to the first source wiring through a source via-hole, and

wherein the second drain wiring is disposed perpendicularly to the lower layer wiring, and connects to the first drain wiring through a drain via-hole.

3. The semiconductor equipment according to claim 1,

wherein the first drain wiring has a minimum width of the stripe, which is narrower than that of the first source wiring.

4. Semiconductor equipment comprising:

a semiconductor substrate;

a plurality of lateral type metal oxide semiconductor transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a mesh pattern; and

upper and lower layer wirings disposed on the substrate for electrically connecting the source cells and the drain cells,

wherein the lower layer wiring includes a first drain wiring for connecting the neighboring two drain cells disposed in a diagonal

direction of the mesh pattern, and a first source wiring for connecting the source cells and surrounding the first drain wiring,

wherein the upper layer wiring includes a second source wiring disposed perpendicularly to the first source wiring and having a plurality of stripes for connecting to the first source wiring through a source via-hole, and a second drain wiring disposed perpendicularly to the first drain wiring and having a plurality of stripes for connecting to the first drain wiring through a drain via-hole,

wherein the second source wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first source wiring disposed between the neighboring first drain wirings, and the second drain wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first drain wiring, and

wherein the stripes of the second source wiring and the second drain wiring are disposed alternately.

5. The semiconductor equipment according to claim 4,

wherein the source cell is disposed on a periphery of the mesh pattern, and the source and drain cells are disposed alternately in an inner mesh pattern,

wherein the first drain wiring is composed of a first type drain wiring and a second type drain wiring,

wherein the first type drain wiring does not connect the drain cell adjacent to the source cell disposed on the periphery of the mesh pattern, and connects the neighboring two drain cells disposed in the diagonal direction of the mesh pattern, and

wherein the second type drain wiring connects the neighboring two, three or four drain cells, which are disposed in the diagonal direction of the mesh pattern and include the drain cell adjacent to the source cell disposed on the periphery of the mesh pattern.

6. The semiconductor equipment according to claim 4,

wherein the minimum width of the stripe of the first drain wiring is narrower than that of the first source wiring disposed between the neighboring two first drain wirings.

7. Semiconductor equipment comprising:

a semiconductor substrate;

a plurality of lateral type metal oxide semiconductor transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a mesh pattern; and

upper and lower layer wirings disposed on the substrate for electrically connecting the source cells and the drain cells,

wherein the lower layer wiring includes a first source wiring for connecting the neighboring two source cells disposed in a diagonal direction of the mesh pattern, and a first drain wiring for connecting the drain cells and surrounding the first source wiring,

wherein the upper layer wiring includes a second source wiring disposed perpendicularly to the first source wiring and having a plurality of stripes for connecting to the first source wiring through a source via-hole, and a second drain wiring disposed

perpendicularly to the first drain wiring and having a plurality of stripes for connecting to the first drain wiring through a drain via-hole,

wherein the second source wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first source wiring disposed between the neighboring first drain wirings, and the second drain wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first drain wiring, and

wherein the stripes of the second source wiring and the second drain wiring are disposed alternately.

8. The semiconductor equipment according to claim 7,

wherein the drain cell is disposed on a periphery of the mesh pattern, and the source and drain cells are disposed alternately in an inner mesh pattern,

wherein the first source wiring is composed of a first type source wiring and a second type source wiring,

wherein the first type source wiring does not connect the source cell adjacent to the drain cell disposed on the periphery of the mesh pattern, and connects the neighboring two source cells disposed in the diagonal direction of the mesh pattern, and

wherein the second type source wiring connects the neighboring two, three or four source cells, which are disposed in the diagonal direction of the mesh pattern and include the source cell adjacent to the drain cell disposed on the periphery of the mesh pattern.

9. The semiconductor equipment according to claim 7,

wherein the minimum width of the stripe of the first drain wiring disposed between the neighboring two first source wirings is narrower than that of the first source wiring.

10. The semiconductor equipment according to claim 1,

wherein each of the second source and drain wirings includes a plurality of stripe portions as a tooth of comb and a connection portion as a body of comb for connecting the stripe portions, and

wherein the stripe portion of the second source wiring faces the stripe portion of the second drain wiring.

11. The semiconductor equipment according to claim 10,

wherein each of the second source and drain wirings further includes a pad for forming a solder bump.

12. The semiconductor equipment according to claim 1, the equipment further comprising:

a third layer wiring disposed on the upper and lower layer wirings,

wherein the third layer wiring includes a third source wiring for connecting to the second source wiring and a third drain wiring for connecting to the second drain wiring, and

wherein each of the third source and drain wirings includes a pad for forming a solder bump.

13. The semiconductor equipment according to claim 2,

wherein at least one of the source and drain via-holes disposed

in a contact portion between the first and second source wirings or between the first and second drain wirings has a plurality of small via-holes.

14. The semiconductor equipment according to claim 2,

wherein at least one of the source and drain via-holes disposed in a contact portion between the first and second source wirings or between the first and second drain wirings has a ring shape.

15. The semiconductor equipment according to claim 2,

wherein at least one of the source and drain via-holes disposed in a contact portion between the first and second source wirings or between the first and second drain wirings has a tapered sidewall.

16. Semiconductor equipment comprising:

a semiconductor substrate;

a plurality of transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a mesh pattern;

a lower layer wiring disposed on the source and drain cells and including a first source wiring for connecting the source cells and a first drain wiring for connecting the drain cells; and

an upper layer wiring disposed on the lower layer wiring and including a second source wiring for connecting to the first source wiring through a source via-hole and a second drain wiring for connecting to the first drain wiring through a drain via-hole,

wherein at least one of the source and drain via-holes has

a predetermined pattern so that a length of periphery of the via-hole becomes maximum.

17. The semiconductor equipment according to claim 16, wherein at least one of the source and drain via-holes has a plurality of small via-holes.

18. The semiconductor equipment according to claim 16, wherein at least one of the source and drain via-holes has a ring shape.